EECS 115 INTRODUCTION TO VLSI
(Required for CpE; Elective for EE)

Catalog Data: **EECS 115 Introduction to VLSI (Credit Units: 4)** A first course in the design of Very Large Scale Integrated (VLSI) systems and chips. Review of CMOS VLSI technology. Analysis and synthesis of basic and complex CMOS gates. Introduction to CAD methodology and usage of CAD Tools. Prerequisite: EECS112/CSE132. Same as CSE151. Formerly ECE151. (Design units: 4)

Textbook: Rabaey, Jan M., *Digital Integrated Circuits: A Design Perspective,* Prentice Hall, 1999.

References: Weste and Eshraghian, *Principles of CMOS VLSI,* 2nd edition, Addison-Wesley.

Coordinator: Fadi Kurdahi

Course Objectives:
To understand the analysis and design of digital integrated circuits.
To acquire working knowledge of area, performance and optimization principles and design tradeoffs of VLSI layouts.
To gain working knowledge of layout design and analysis CAD tools.
To understand the issues and concepts governing the design, implementation and fabrication and the impact of processing technology on the scaling of digital ICs.

Course Outcomes:
Students will:
Design circuits that perform combinational and sequential functions and analyze their performance when implemented in ICs.
Design VLSI layouts, analyze, and optimize or tradeoff their quality metrics given a set of constraints.

Prerequisites By Topic:
Building blocks and organization of digital computers.
Arithmetic, control and memory units.
Input/out devices and interfaces.
Microprogramming and microprocessors.

Lecture Topics:
Introduction.
Review, diode, MOSFET Static and dynamic behavior.
Inverter, Static CMOS and Dynamic CMOS.
Combinational Logic Design.
Design of Sequential Circuits.
Design of Arithmetic Building Block.
Timing Issues.

Class Schedule: Meets for 3 hours of lecture and 1 hour of discussion each week for 10 weeks.

Computer Usage: MAGIC, IRSIM, SPICE (or equivalent).

Laboratory Projects: Spice simulation, layout for inverter, layout for oscillator, layout for adder.

Professional Component: Contributes toward the Computer Engineering Topics Courses and Major Design experience.

Relationship to Program Outcomes: This course relates to Program Outcomes a, b, c, e, j and k as stated at: http://undergraduate.eng.uci.edu/degreeprograms/computer/mission

Design Content Description

Approach: Study of devices; diode, transistor, NMOS and PMOS; and the design of: Inverter, Combinational, Clock screw, ALU, Memory.
Lectures: 50%
Laboratory Portion: 50%

Grading Criteria:

Home work:	10%
Projects:	35%
Midterm Exam:	25%
Final Exam:	30%
	100%

Estimated ABET Category Content:

Mathematics and Basic Science: 0 credit units or 0%
Engineering Science: 0 credit units or 0%
Engineering Design: 4 credit units or 100%

Prepared by: Fadi Kurdahi **Date:** July 2007

CEP Approved: Fall 2004