

EECS 175B VERY LARGE SCALE INTEGRATION (VLSI) PROJECT TESTING
(Elective for EE)

Catalog Data:	EECS 175B Very Large Scale Integration (VLSI) Project Testing (Credit Units: 4) Test and document student-created Complementary Metal Oxide Semiconductor (CMOS) Very Large Scale Integration (VLSI) projects designed in EECS175A. Emphasis on practical laboratory experience in VLSI testing techniques. Prerequisite: EECS175A or consent of instructor. Concurrent with EECS275B. Formerly 115B. (Design units: 0)
Textbook:	
References:	Weste, Eshraghan, and Smith, <i>Principles of CMOS VLSI Design</i> , and/or other equivalent books will be suggested as reference textbooks. List of recent publications that are indicative of the type of projects students may undertake will be provided as references.
Coordinator:	Stuart Kleinfelder
Course Objectives:	Test and document the VLSI designs made in EECS175A.
Course Outcomes:	Students will: Apply their creativity and experience in the selection of a VLSI design project of appropriate breadth and depth. Understand and use analog and/or digital CMOS design as appropriate for their chosen project. Use VLSI design tools to design large and complex CMOS circuits, including full custom layout techniques. Simulate and verify large and complex VLSI circuits to demonstrate the correctness of their project. Complete the submission process for the fabrication of their CMOS VLSI project.
Prerequisites By Topic:	Excellent understanding of CMOS VLSI design principles and techniques. General electronic laboratory skills.
Lecture Topics:	Lectures will include practical guidance on the use of specialized test hardware and test techniques. Frequent in-class reviews of student projects will take place in order to monitor progress and provide guidance.
Class Schedule:	Meets for 3 hours of lecture and 3 hour of lab each week for 10 weeks.
Computer Usage:	Computers and computer aided design software will be used as needed to compare simulation and actual test results.
Laboratory Projects:	Test completed VLSI design projects from EECS175A using specialized chip testing pattern generators and logic analyzers, etc.
Professional Component:	

Relationship to Program Outcomes: This course relates to Program Outcomes a, b, c, d, e, f, g, h, i, j, and k as stated at:

<http://undergraduate.eng.uci.edu/degreeprograms/electrical/mission>

Design Content Description

Approach:

Lectures:

Laboratory Portion:

Grading Criteria:

The testing program plan quality and scope:	30%
Completeness of design testing:	40%
Completeness and quality of the test documentation:	<u>30%</u>
	100%

An additional requirement for graduate students will be an oral presentation and defense of their work, which will provide a basis for a grading differentiation between graduate and undergraduate students.

Estimated ABET Category Content:

Mathematics and Basic Science: 0 credit units or 0%

Engineering Science: 4 credit units or 100%

Engineering Design: 0 credit units or 0%

Prepared by: Stuart Kleinfelder **Date:** July 2007

CEP Approved: Fall 2005